

AMENDMENTS TO THE CLAIMS

Claims 1-9 (Canceled)

¹
Claim ¹10 (Previously Presented): An apparatus for processing data in a spread spectrum system, comprising:

a decimation circuit having an associated decimation factor;

a memory, which is a single port RAM, coupled to said decimation circuit, wherein said memory is divided into memory blocks such that during processing a first subset of memory blocks is in a Read mode and a second subset of memory blocks is in a Write mode; and

an interpolation circuit coupled to said memory, said interpolation circuit having an associated interpolation factor;

wherein said decimation circuit decimates a data rate of received data by said decimation factor to a decimated rate and stores said received data into said memory at said decimated rate; and

wherein said interpolation circuit interpolates said decimated rate by said interpolation factor to an interpolated rate and retrieves said received data from said memory at said interpolated rate.

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Claim ¹11 (Original): The apparatus of claim ¹10, further comprising a plurality of despreaders.

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Claim ²12 (Original): The apparatus of claim ¹11, wherein each of said plurality of despreaders includes:

a selector circuit; and

a rake finger.

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Claim ³13 (Original): The apparatus of claim ²12, wherein each of said memory blocks are divided into segments such that data stored in each segment is read out sequentially onto a bussing element accessible by multiple rake fingers via selector circuits in said plurality of despreaders.

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Claim 14 (Original): The apparatus of claim 12, wherein said selector circuit includes a block multiplexer, a plurality of sample multiplexers, and a cache coupled to each rake finger.

Claims 15-19 (Canceled)

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Claim 20 (Previously Presented): An apparatus for processing data in a spread spectrum system, comprising:

a decimation circuit having an associated decimation factor;

a memory, which is a circular buffer including multiple registers, coupled to said decimation circuit;

an interpolation circuit coupled to said memory, said interpolation circuit having an associated interpolation factor; and

a plurality of despreaders, wherein each of said plurality of despreaders includes:

a selector circuit; and

a rake finger;

wherein said decimation circuit decimates a data rate of received data by said decimation factor to a decimated rate and stores said received data into said memory at said decimated rate;

wherein said interpolation circuit interpolates said decimated rate by said interpolation factor to an interpolated rate and retrieves said received data from said memory at said interpolated rate; and

wherein said selector circuit includes a first set of multiplexers for selecting in-phase data, a second set of multiplexers for selecting quadrature data, and multiple sample select lines coupled to each rake finger.

Claims 21-23 (Canceled)

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Claim 24 (Original): An apparatus for processing data, comprising:

a plurality of rake fingers;

a memory for storing data at the input to said plurality of rake fingers; and

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a selector circuit positioned between said memory and each of said plurality of rake fingers;
wherein said plurality of rake fingers can access said memory substantially simultaneously
via a respective selector circuit, and

wherein said selector circuit includes a first plurality of multiplexers for selecting in-phase data from said memory, a second plurality of multiplexers for selecting quadrature data from said memory, and a set of select lines for controlling data being selected by said first plurality of multiplexers and said second plurality of multiplexers.

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Claim ~~25~~²⁵ (Original): The apparatus of claim ~~24~~⁷, wherein said memory is a circular buffer including a plurality of registers.

Claim 26 (Canceled)

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Claim ~~27~~²⁷ (Original): The apparatus of claim ~~24~~⁷, wherein said memory is a single-port RAM.

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Claim ~~28~~²⁸ (Previously Presented): An apparatus for processing data, comprising:

a plurality of rake fingers;

a memory, which is a single-port RAM, for storing data at the input to said plurality of rake fingers; and

a selector circuit positioned between said memory and each of said plurality of rake fingers;

wherein said plurality of rake fingers can access said memory substantially simultaneously via a respective selector circuit; and

wherein said memory is divided into memory blocks such that, during each processing cycle, a first subset of said memory blocks is in a Read mode and a second subset of said memory blocks is in a Write mode.

¹¹
Claim ~~29~~²⁹ (Original): The apparatus of claim ~~28~~¹⁰, wherein each of said memory blocks is divided into segments, such that data stored in each segment is read out sequentially onto a bussing element.

¹²
Claim 30 (Original): The apparatus of claim ¹¹~~29~~, wherein said selector circuit includes a block multiplexer, a plurality of sample multiplexers, and a cache coupled to each rake finger.

¹³ Claim ~~31~~ (Original): The apparatus of claim ¹² ~~30~~, wherein said block multiplexer selects a bussing element to receive data from a segment.

Claim ¹⁴32 (Original): The apparatus of claim ¹³31, wherein said sample multiplexers selects data received from said block multiplexer and stores said data into said cache.

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Claim 33 (Original): An apparatus for processing data in spread spectrum systems, comprising:
a memory coupled to a set of despreaders via a bus;
each of said set of despreaders including:
a block multiplexer coupled to said bus;
a set of sample multiplexers coupled to said block multiplexer;
a cache coupled to said sample multiplexers; and
a rake finger coupled to said cache; and
wherein said set of despreaders can access samples stored in said memory substantially simultaneously via said bus.

Claim ¹⁶34 (Original): The apparatus of claim ¹⁵33, wherein said memory is divided into blocks such that during a processing cycle by a despreaders, a first subset of said blocks is in a Read mode and a second subset of said blocks is in a Write mode.

¹⁷Claim ~~35~~ (Original): The apparatus of claim ¹⁶~~34~~, wherein said blocks are divided into segments such that samples stored in each of said segments are read out sequentially onto a bussing element coupled to said bus.

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Claim 36 (Original): The apparatus of claim 35, wherein said block multiplexer in each of said
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despreaders selects samples from one bussing element.

¹⁹Claim-~~37~~ (Original): The apparatus of claim ¹⁸~~36~~, wherein said sample multiplexers in each of said despreaders select appropriate Early, On-Time, and Late samples among samples received from said block multiplexer to be stored into said cache.